WHAT IS CLAIMED IS:

1. A COC device comprising:

a logic chip having a logic circuit;

a memory chip mounted on the logic chip, the memory chip comprising: basic chips functioning as a chip independently from each other; and a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip; and

a bump connecting the logic chip and the memory chip.

2. The COC device according to claim 1, wherein the basic chips have all the same layout.

3. The COC device according to claim 1, wherein a part of the basic chips has a layout inverting a layout of another part of the basic chips.

4. The COC device according to claim 1, wherein the dicing line is formed with at least one of an alignment mark and a test element group.

5. The COC device according to claim 1, wherein in the case where the basic chips are square, one side of individual basic chips has a length of 2 mm or more.

6. The COC device according to claim 5, wherein the dicing line has a width of 0.1 mm.

7. The COC device according to claim 1, wherein the basic chips have a bump.

8. The COC device according to claim 1, wherein the basic chips have a circuit capable of changing a word organization by a control signal.

9. A COC device comprising:

a logic chip having a logic circuit;

a memory chip mounted on the logic chip, the memory chip comprising: basic chips functioning as a chip independently from each other, and capable of changing a word organization by a control signal; and a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip; and

a bump connecting the logic chip and the memory chip;

wherein the control signal is supplied from the logic chip to the memory chip.

10. The COC device according to claim 9, wherein the basic chips have all the same layout.

11. The COC device according to claim 9, wherein a part of the basic chips has a layout inverting a layout of another part of the basic chips.

12. The COC device according to claim 9, wherein the dicing line is formed with at least one of an alignment mark and a test element group.

13. The COC device according to claim 9, wherein in the case where the basic chips are square, one side of individual basic chips has a length of 2 mm or more.

14. The COC device according to claim 13, wherein the dicing line has a width of 0.1 mm.

15. The COC device according to claim 9, wherein the basic chips have a bump.

16. A SiP device comprising:

a COC device according to claim 1; and

a package covering said COC device.

17. A SiP device comprising:

a COC device according to claim 9; and

a package covering said COC device.